



# TGA2237-SM

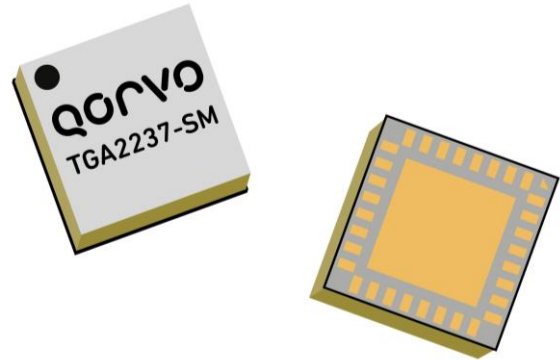
## 0.03–2.5 GHz 10 W GaN Power Amplifier

### Product Overview

Qorvo's TGA2237-SM is a wideband distributed amplifier fabricated on Qorvo's production 0.25  $\mu\text{m}$  GaN on SiC process. The TGA2237-SM operates from 0.03–2.5 GHz and provides greater than 10 W of saturated output power with greater than 13 dB of large signal gain and greater than 50% power-added efficiency.

The TGA2237-SM is available in a low-cost, surface mount 32 lead 5 x 5 laminated QFN. It is ideally suited to support both radar and communication applications across defense and commercial markets as well as electronic warfare. The TGA2237-SM is fully matched to 50 $\Omega$  at both RF ports allowing for simple system integration. DC blocks are required on both RF ports and the drain voltage must be injected through an off chip bias-tee on the RF output port.

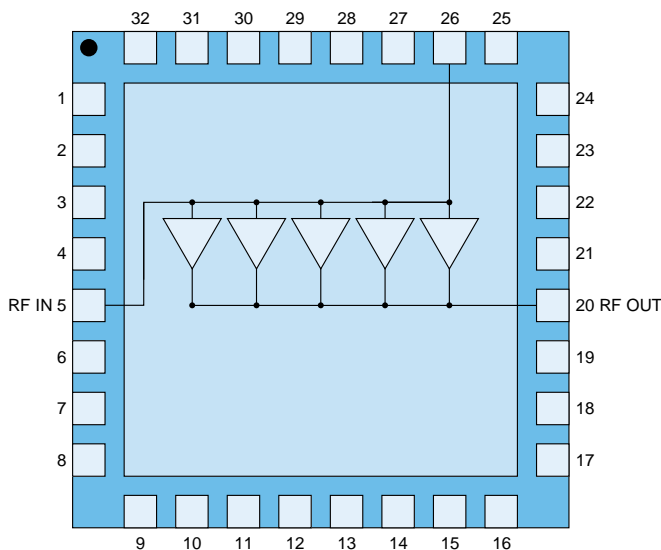
Lead-free and RoHS compliant.



### Key Features

- Frequency Range: 0.03–2.5 GHz
- $P_{\text{SAT}}$ : 40 dBm at  $P_{\text{IN}} = 27$  dBm
- P1 dB: 33 dBm
- PAE: 50%
- Large Signal Gain: 13 dB
- Small Signal Gain: 19 dB
- Input Return Loss: 10 dB
- Output Return Loss: 12 dB
- Bias:  $V_{\text{D}} = 32$  V,  $I_{\text{DQ}} = 360$  mA
- Wideband Flat Power
- Package Dimensions: 5.0 x 5.0 x 1.596 mm

### Functional Block Diagram



Top View

### Applications

- Commercial and Military Radar
- Communications
- Electronic Warfare

### Ordering Information

Part No.	Description
TGA2237-SM	0.03–2.5 GHz 10 W GaN Power Amplifier
TGA2237-SMEVB	Evaluation Board for TGA2237-SM

## Absolute Maximum Ratings

Parameter	Value / Rang
Drain Voltage ( $V_D$ )	40 V
Gate Voltage Range ( $V_G$ )	-8 to 0 V
Drain Current ( $I_D$ )	1.2 A
Gate Current ( $I_G$ )	-2.4 to 8.4 mA
Power Dissipation ( $P_{DISS}$ ), 85 °C	19 W
Input Power ( $P_{IN}$ ), CW, 50 $\Omega$ , 85 °C	33 dBm <sup>(*)</sup>
Input Power ( $P_{IN}$ ), CW, VSWR 3:1, $V_D = 32V$ , 85 °C	33 dBm <sup>(*)</sup>
Max VSWR, CW, $P_{IN} = 27$ dBm, $V_D = 32$ V, 85 °C (Load)	10:1
Mounting Temperature (30 Seconds)	260 °C
Storage Temperature	-55 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

## Recommended Operating Conditions

Parameter	Value / Range
Drain Voltage ( $V_D$ )	32 V
Drain Current ( $I_{DQ}$ )	360 mA

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

(\*) Operational input power must be limited to 26 dBm when operating below 0.6 GHz to prevent excessive forward gate current

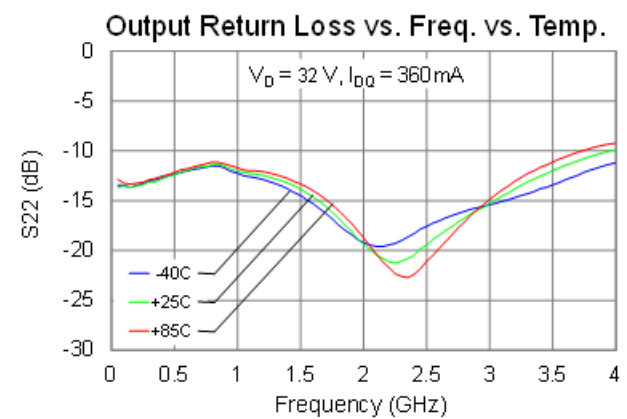
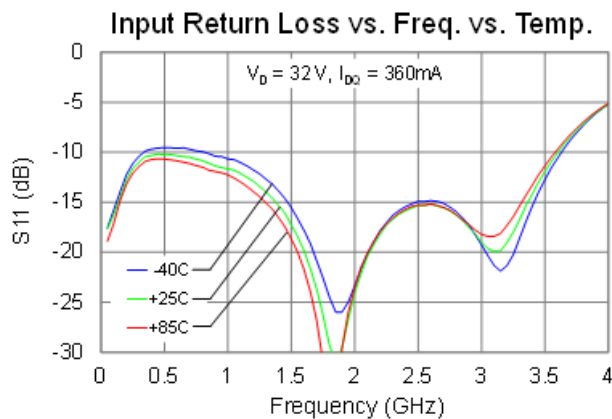
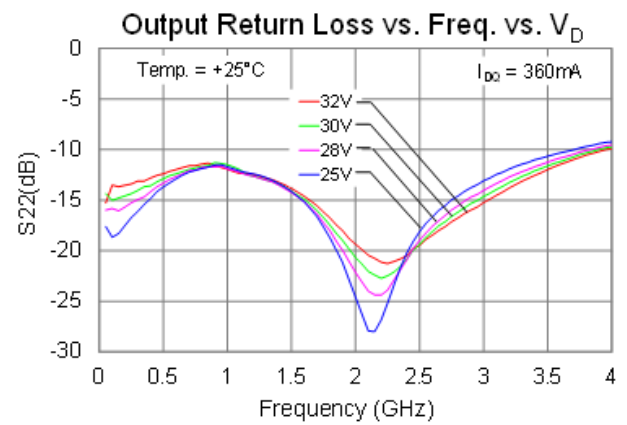
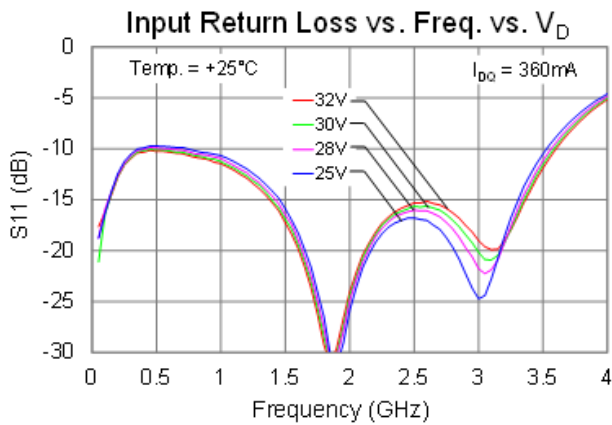
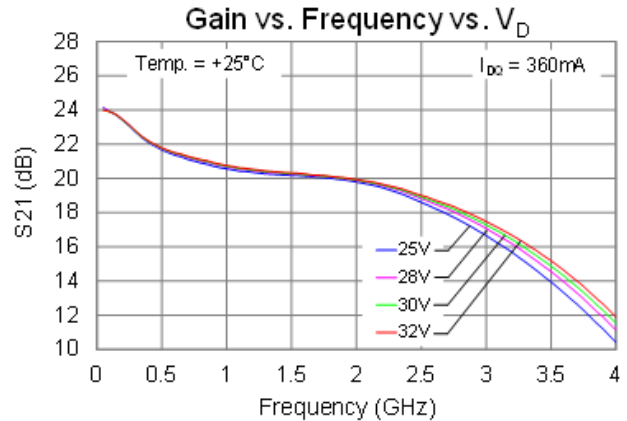
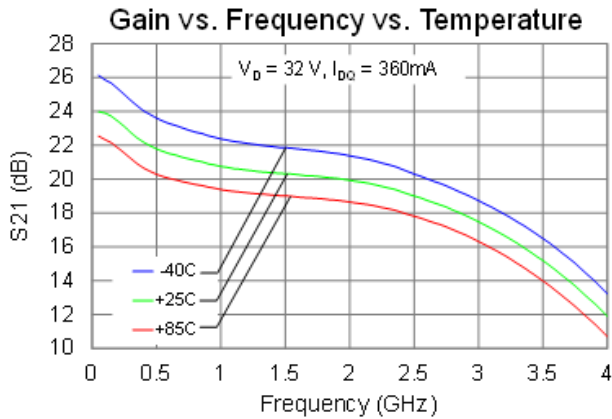
## Electrical Specifications

Parameter	Min	Typ	Max	Units
Operational Frequency Range	0.03		2.5	GHz
Small Signal Gain		19		dB
Input Return Loss		10		dB
Output Return Loss		12		dB
Output Power ( $P_{IN} = 27$ dBm)		40		dBm
Power Added Efficiency ( $P_{IN} = 27$ dBm)		50		%
Power @ 1 dB Compression ( $P_{1dB}$ )		33		dBm
IM3 @ $P_{OUT}/tone = 30$ dBm		-25		dBc
IM5 @ $P_{OUT}/tone = 30$ dBm		-33		dBc
Small Signal Gain Temperature Coefficient		-0.03		dB/°C
Output Power Temperature Coefficient		-0.002		dBm/°C
Recommended Operating Voltage:	20	32		V
Gate Leakage ( $V_D = 10$ V, $V_G = -3.7$ V)	-2.64			mA

Test conditions unless otherwise noted: 25 °C,  $V_D = 32$  V,  $I_{DQ} = 360$  mA

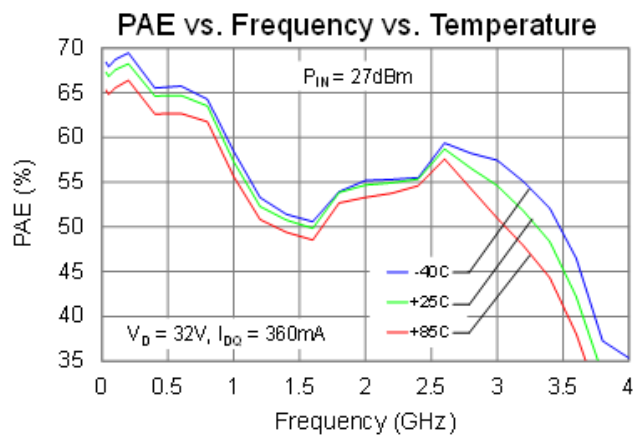
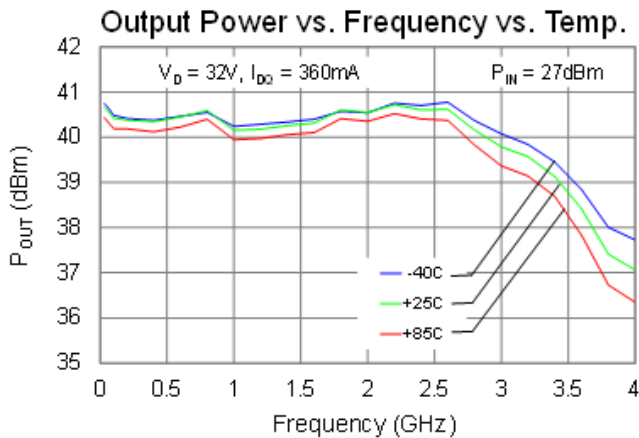
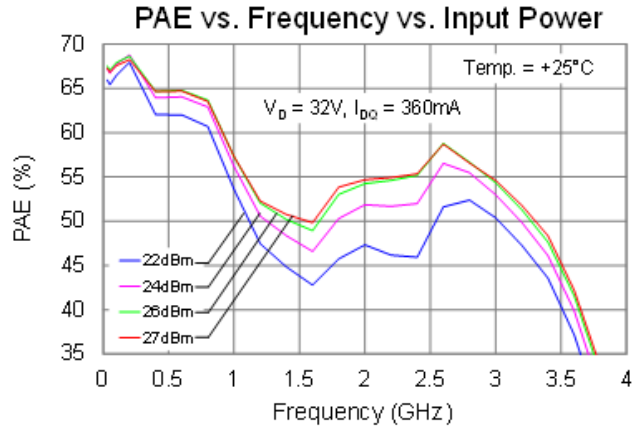
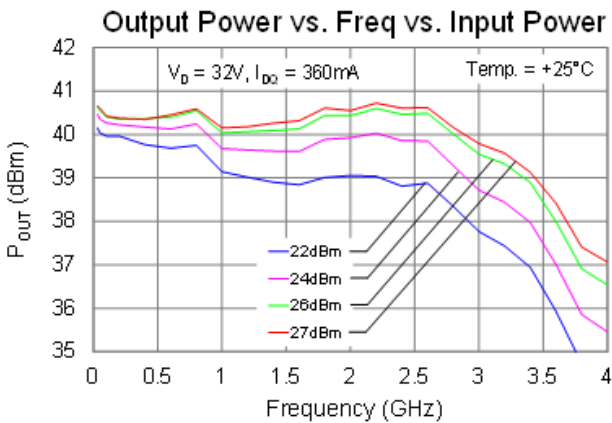
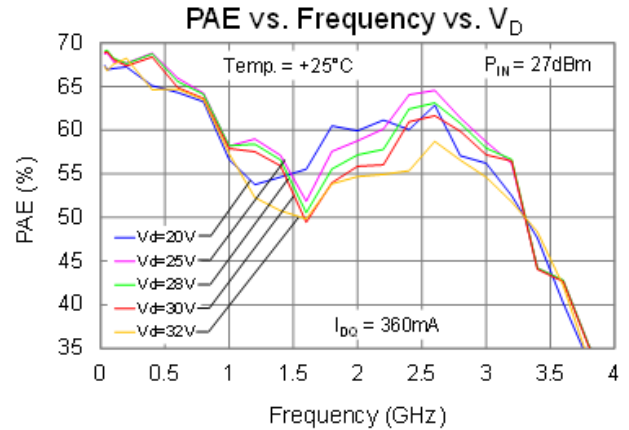
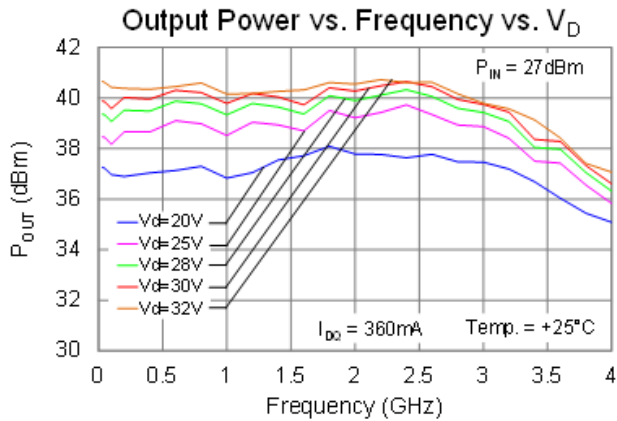
**Performance Plots – Small Signal**

The plots reflect performance measured with an external coaxial bias tee and DC blocks  
 (See application circuit on page 11)



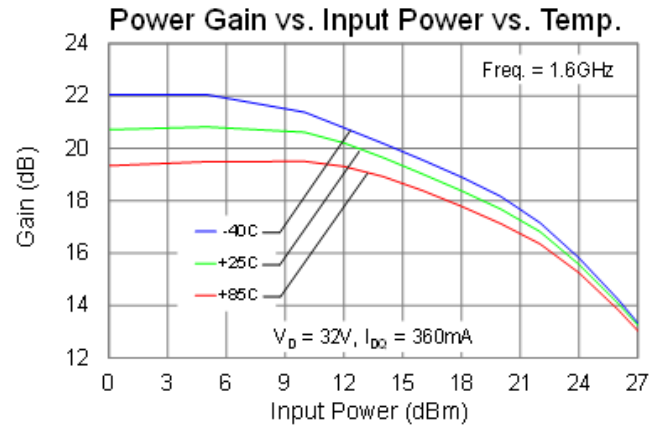
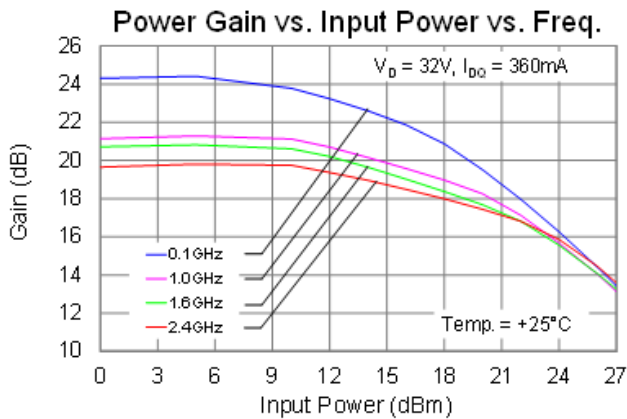
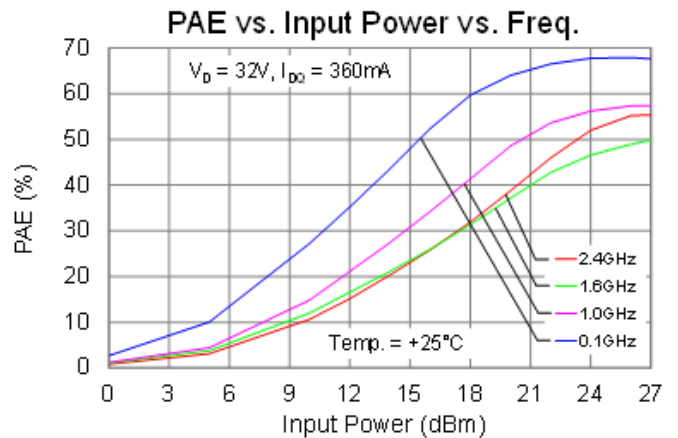
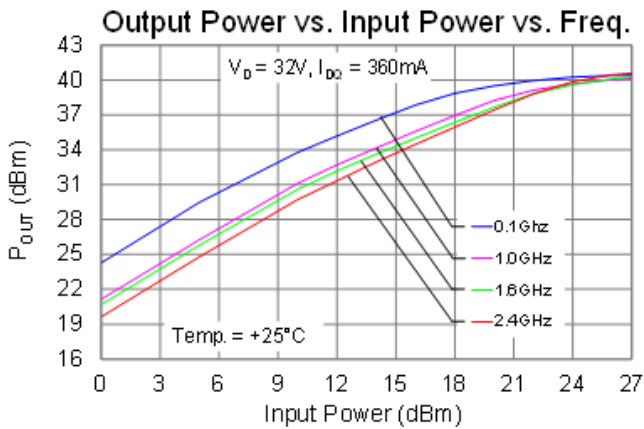
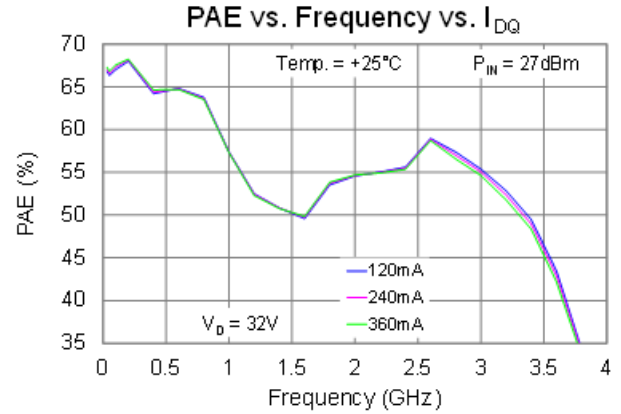
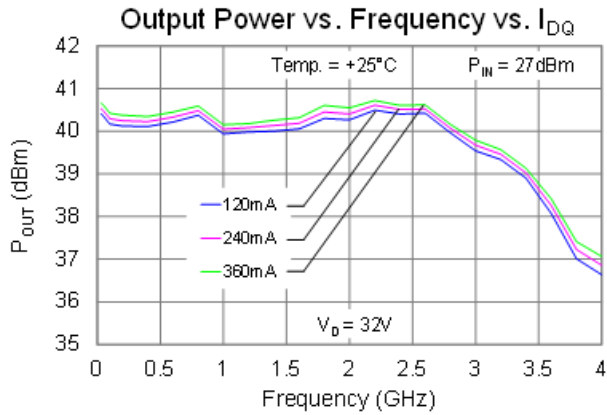
**Performance Plots – Large Signal (CW)**

The plots reflect performance measured with an external coaxial bias tee and DC blocks  
 (See application circuit on page 11)



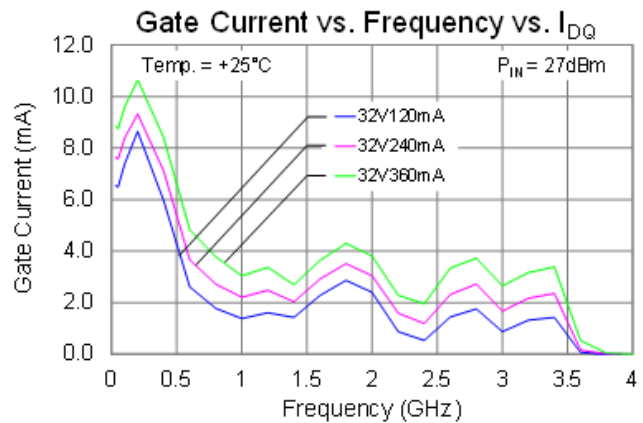
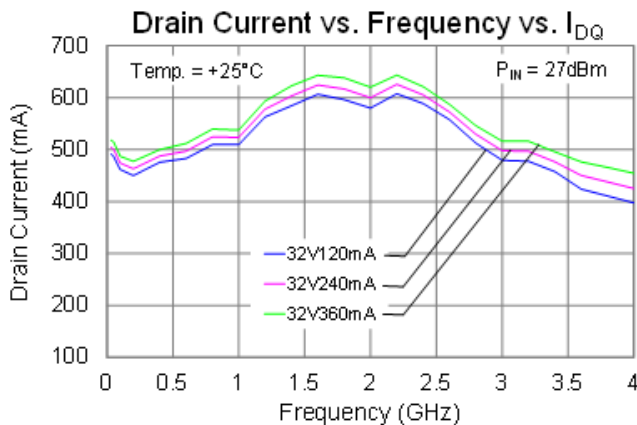
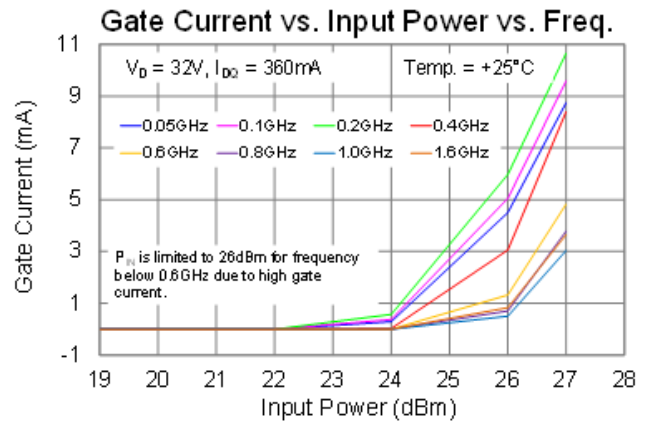
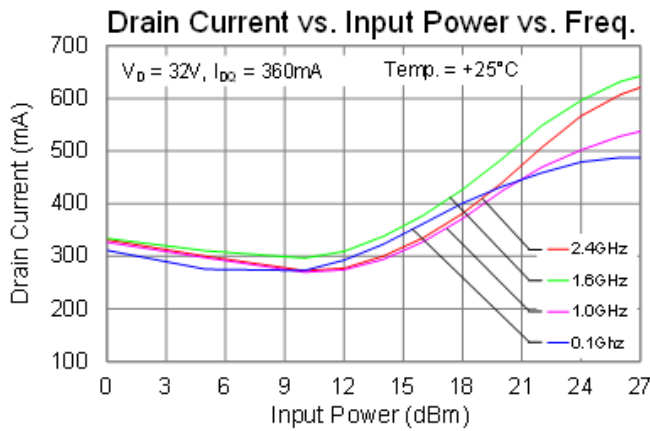
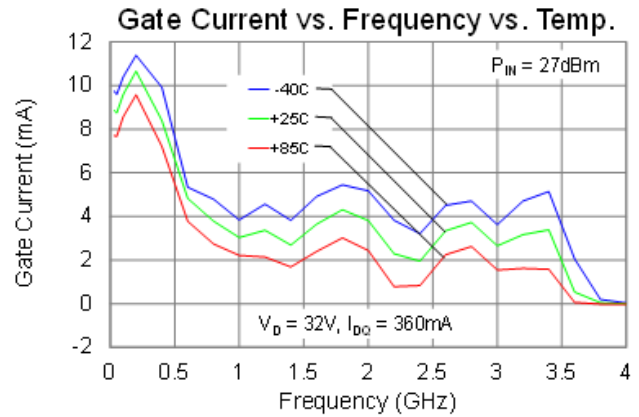
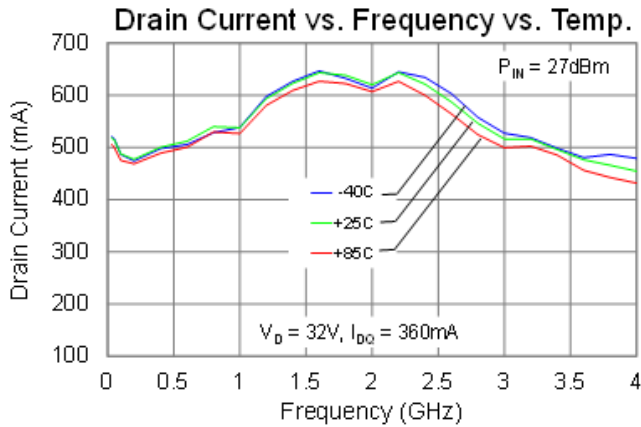
Performance Plots – Large Signal (CW)

The plots reflect performance measured with an external coaxial bias tee and DC blocks  
(See application circuit on page 11)



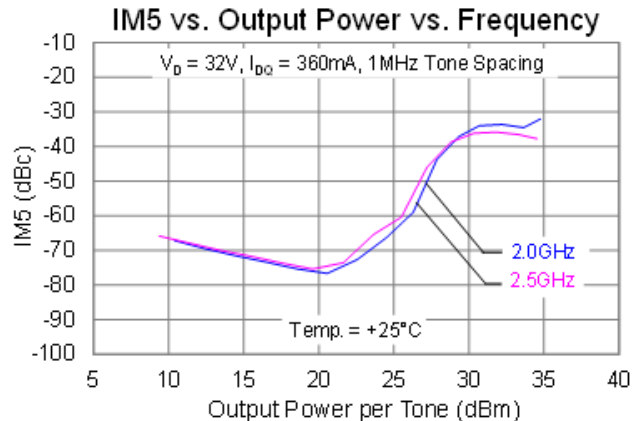
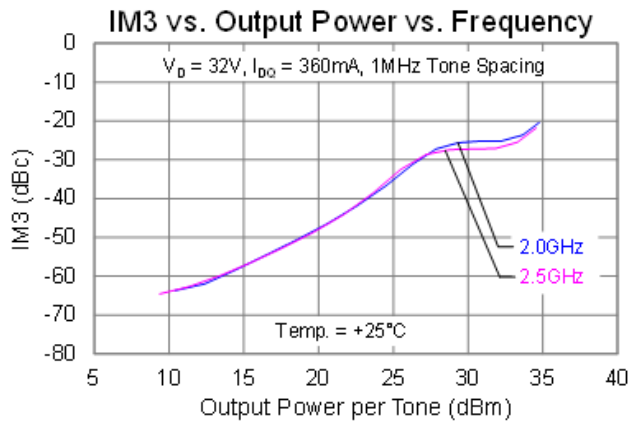
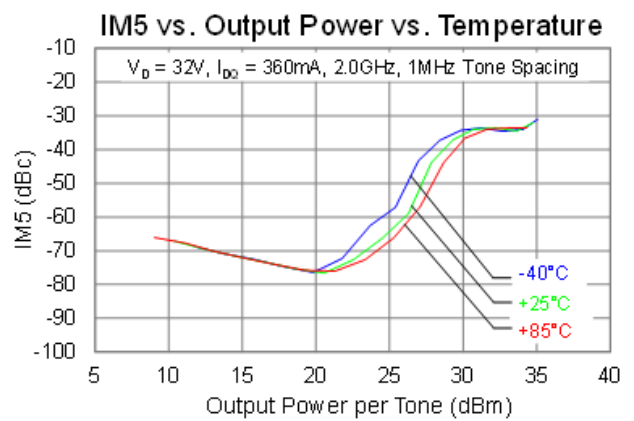
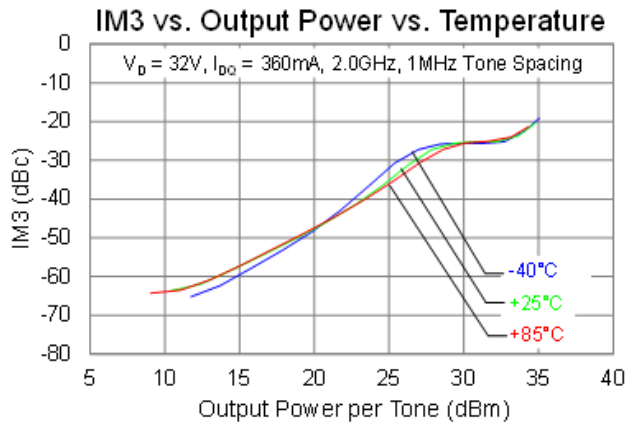
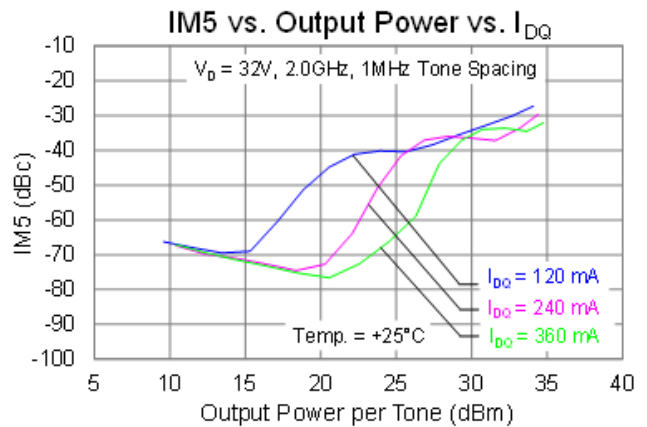
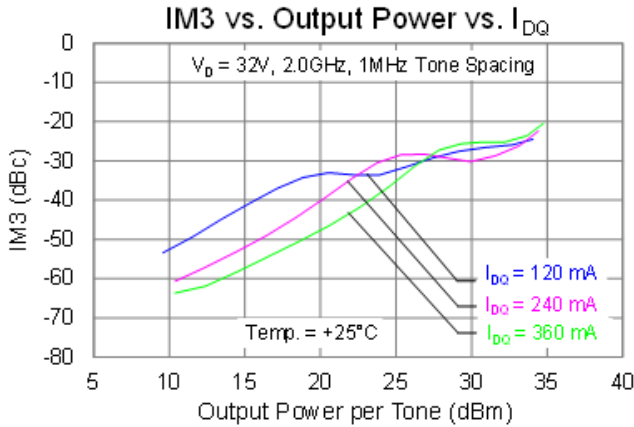
**Performance Plots – Large Signal (CW)**

The plots reflect performance measured with an external coaxial bias tee and DC blocks  
 (See application circuit on page 11)



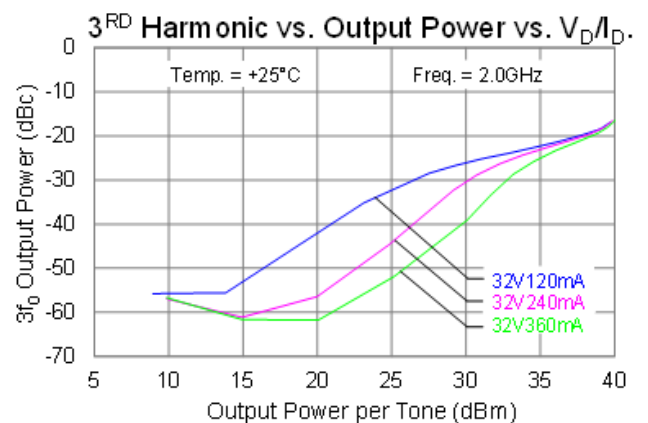
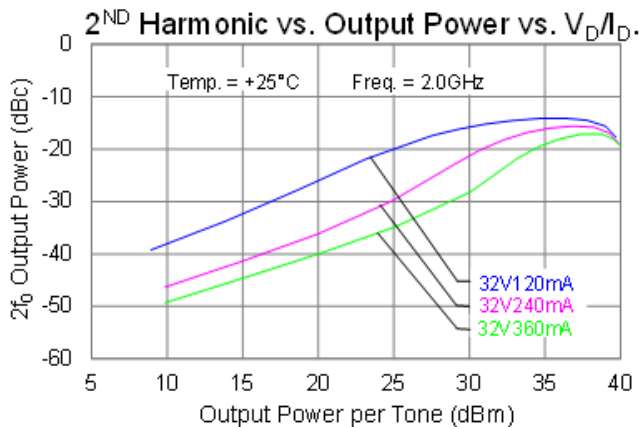
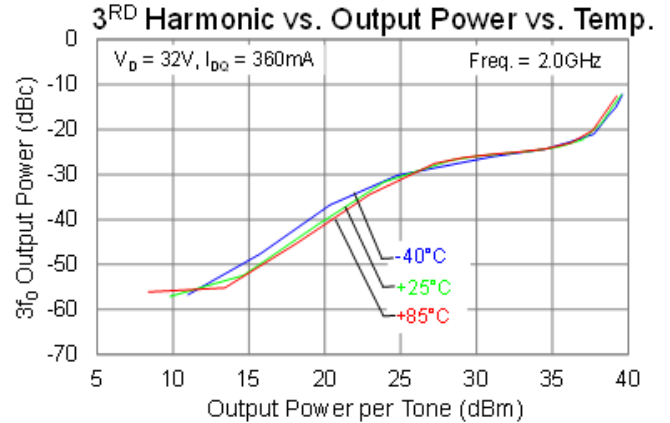
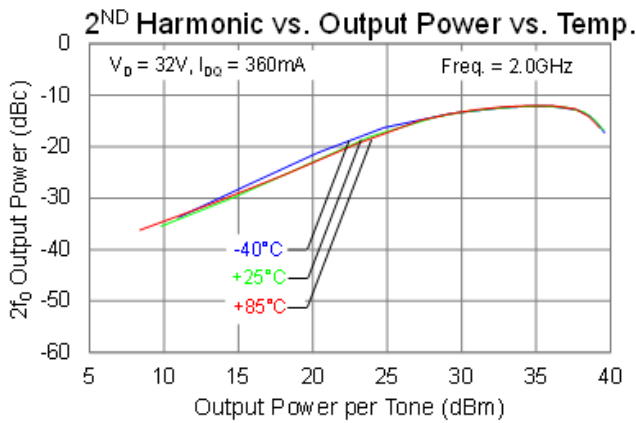
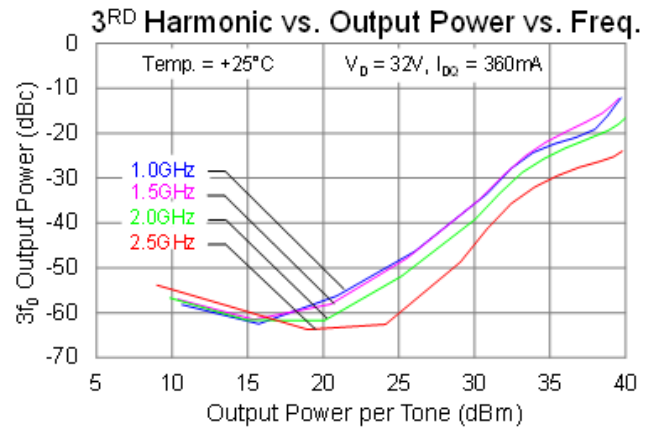
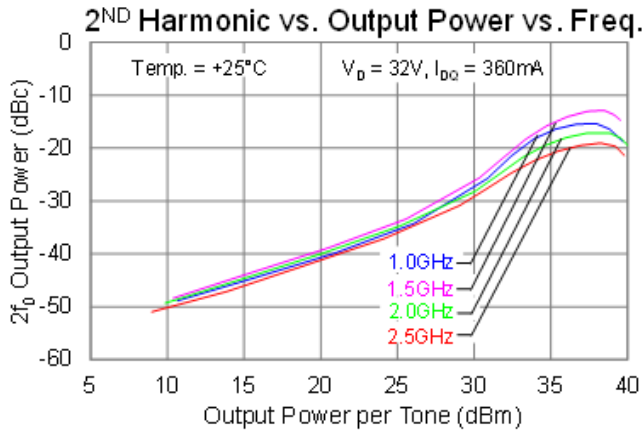
Performance Plots – Linearity

The plots reflect performance measured with an external coaxial bias tee and DC blocks  
(See application circuit on page 11)



Performance Plots – Linearity

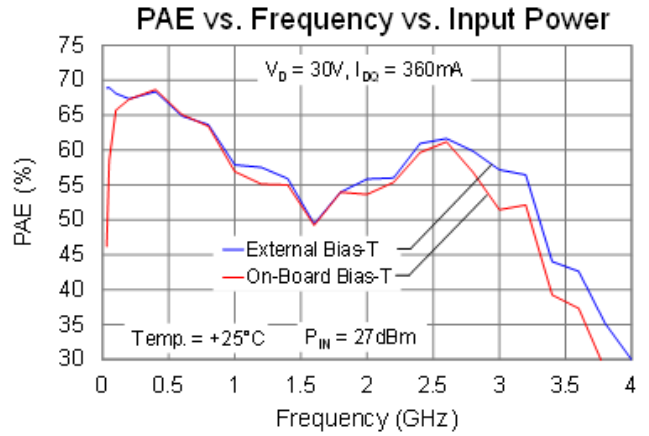
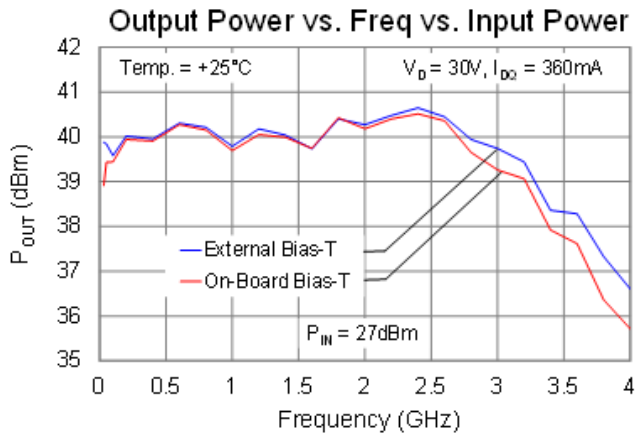
The plots reflect performance measured with an external coaxial bias tee and DC blocks  
(See application circuit on page 11)





Performance Plots – Large Signal (CW), On-board vs. External Coaxial Bias-T

The plots below reflect performance measured between external bias tee and on-board bias tee (See application circuit on pages 11 and 13)



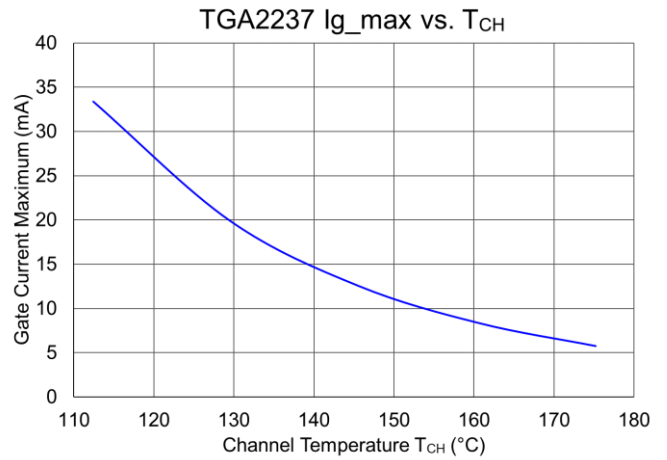
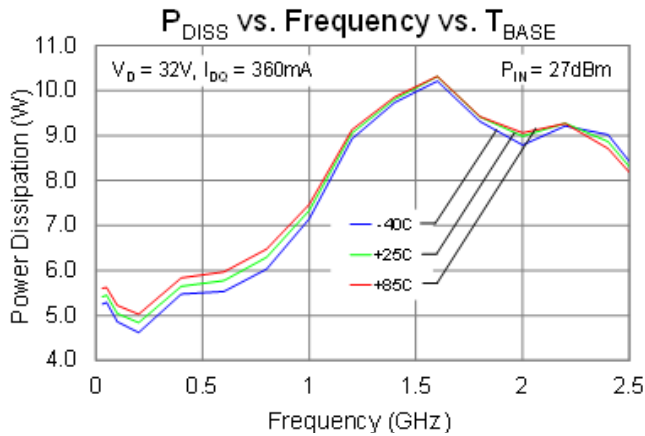
## Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance ( $\theta_{JC}$ ) <sup>(1)</sup>	$T_{base} = 85\text{ }^{\circ}\text{C}$ , $V_D = 32\text{ V}$ , $I_{DQ} = 360\text{ mA}$ , $I_{D\_Drive} = 630\text{ mA}$ , $P_{IN} = 27\text{ dBm}$ , $P_{OUT} = 40\text{ dBm}$ , $P_{DISS} = 10\text{ W}$	6.79	$^{\circ}\text{C/W}$
Channel Temperature ( $T_{CH}$ ) (Under RF drive) <sup>(2)</sup>		152.9	$^{\circ}\text{C}$

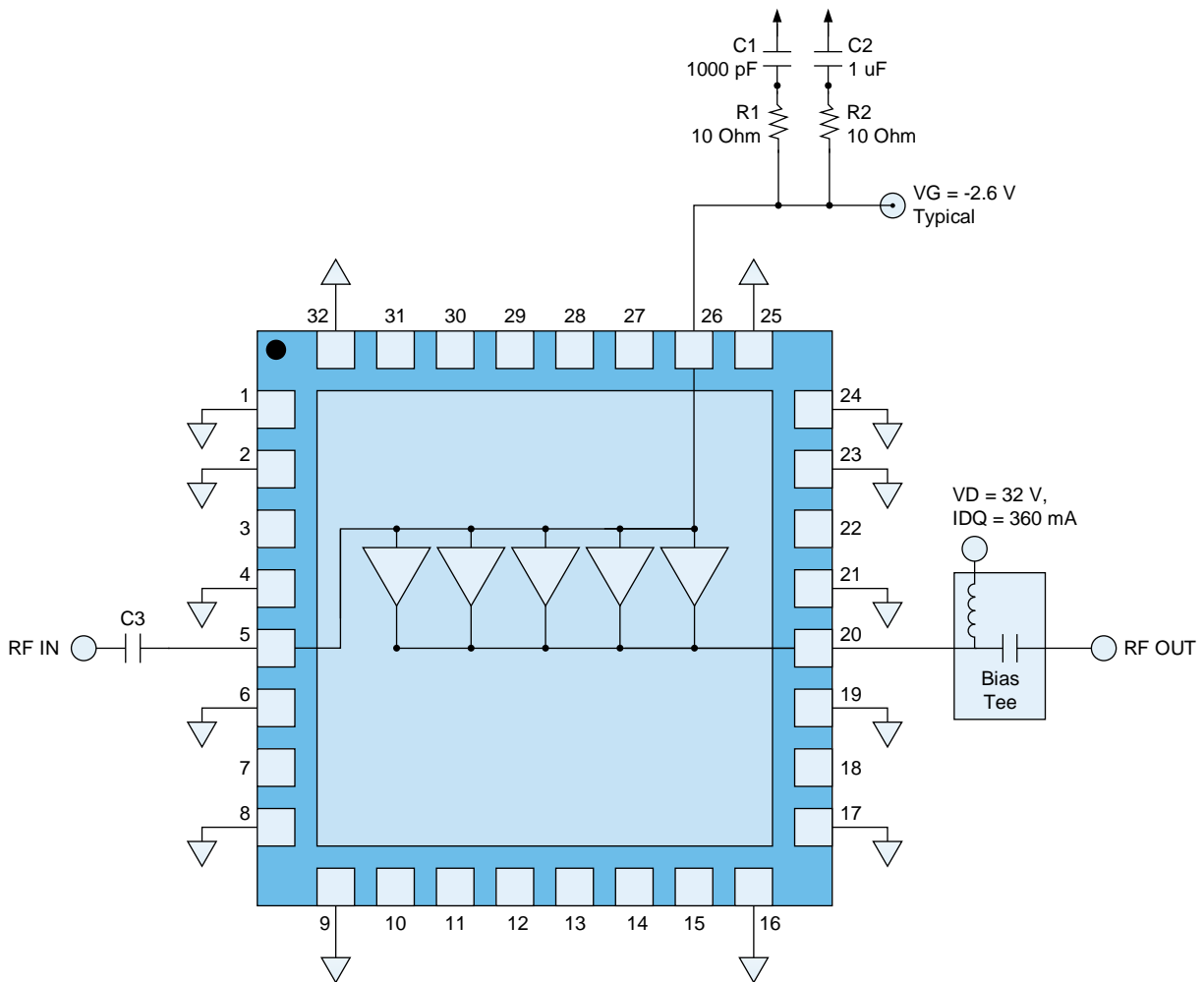
**Notes:**

1. Thermal resistance measured to back of package.
2. Refer to the following document: [GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates](#)

## Dissipated Power and Maximum Gate Current



Application Circuit (Coaxial input DC block and coaxial output bias tee)



Notes:

1. Coaxial input DC block (C3) is used for input port (RF In.)
2. External wide bandwidth Bias-Tee is used for output port (RF Out).  $V_D$  is applied through the output Bias-Tee.

Bias-Up Procedure

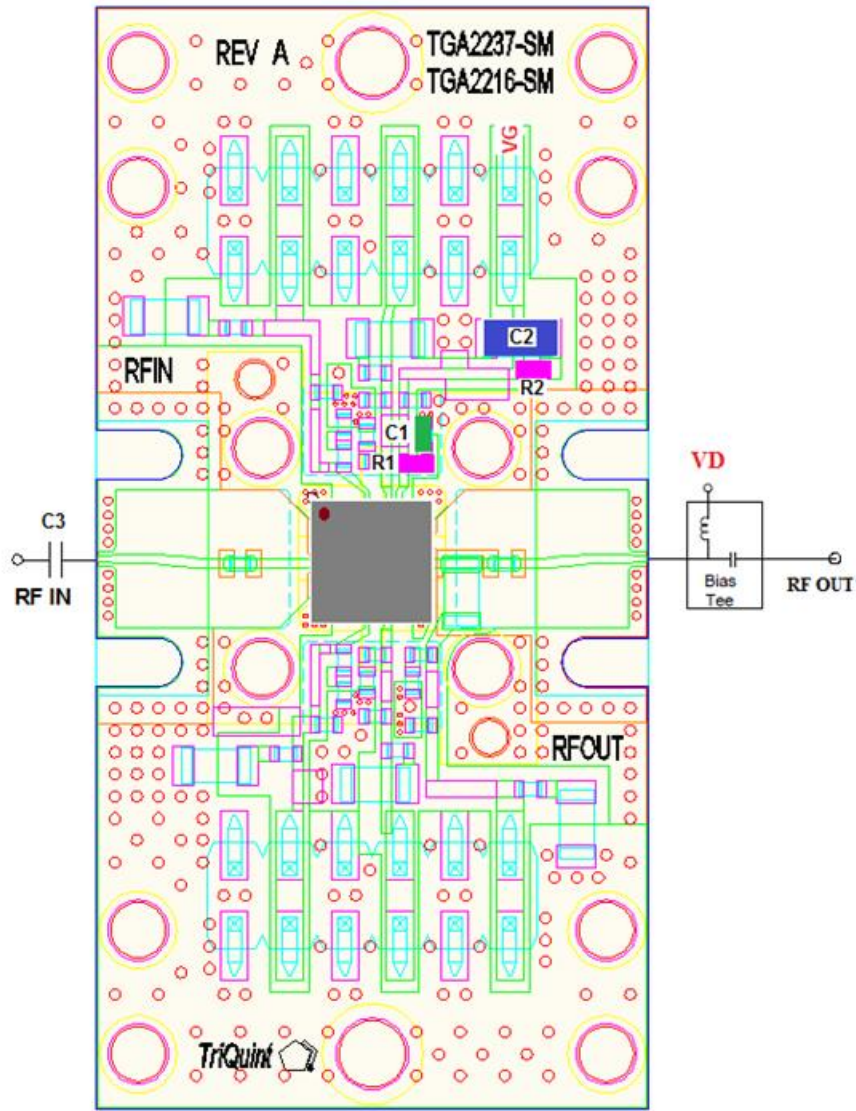
1. Set  $I_D$  limit to 700 mA,  $I_G$  limit to 7 mA
2. Set  $V_G$  to -5.0 V
3. Set  $V_D$  +32 V
4. Adjust  $V_G$  more positive until  $I_{DQ} = 360$  mA
5. Apply RF signal \*

Bias-Down Procedure

1. Turn off RF signal
2. Reduce  $V_G$  to -5.0 V. Ensure  $I_{DQ} \sim 0$  mA
3. Set  $V_D$  to 0 V
4. Turn off  $V_D$  supply
5. Turn off  $V_G$  supply

(\*)  $P_{IN}$  is limited to 26 dBm for frequency < 0.6 GHz due to high gate current.

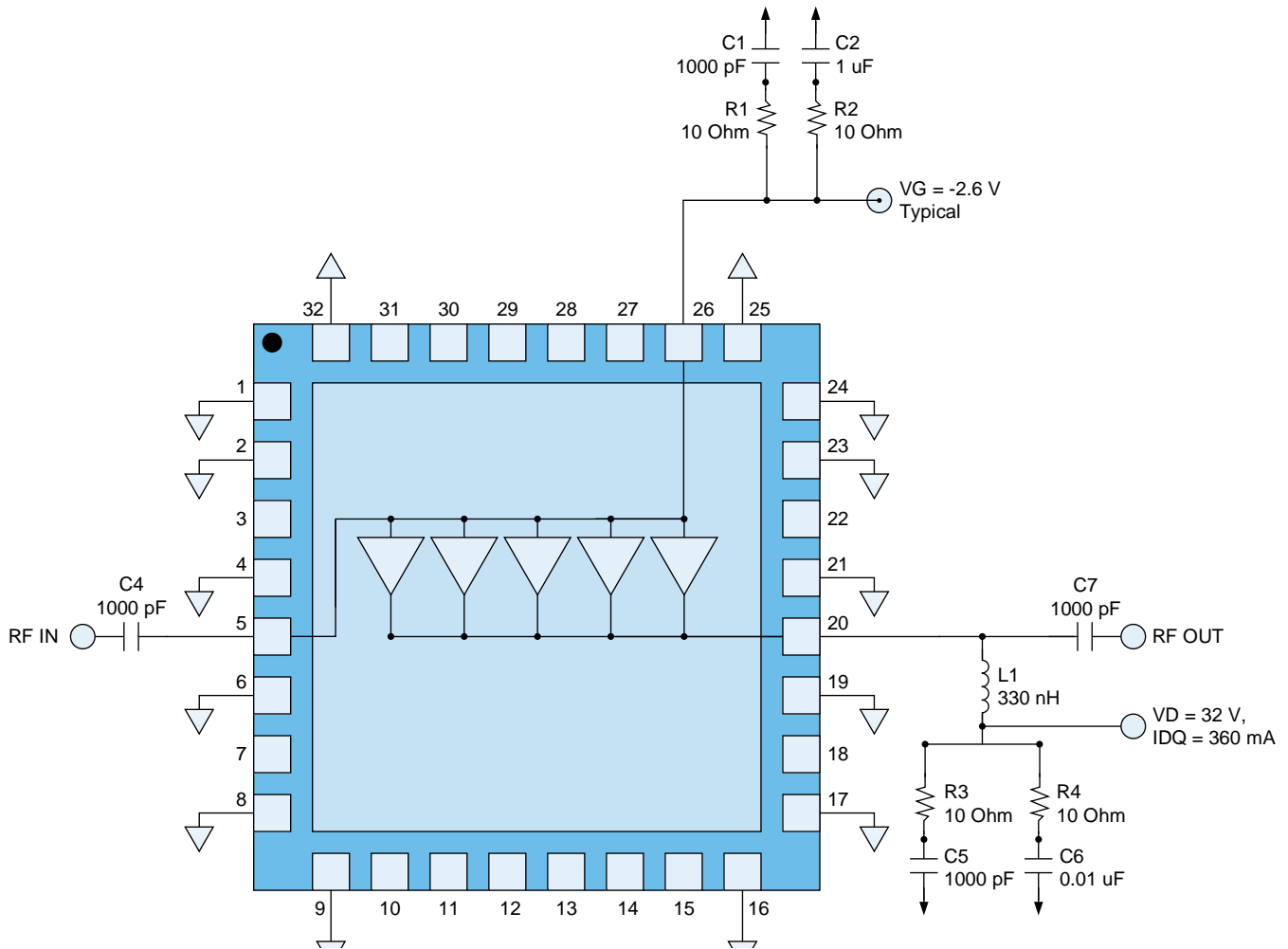
Assembly Drawing (Coaxial input DC block and coaxial output bias tee)



Bill of Materials

Reference Des.	Value	Description	Manuf.	Part Number
C1	1000 pF	Cap, 0402, 100 V, 10%, X7R	Various	
C2	1 uF	Cap, 1206, 50 V, 10%, X7R	Various	
C3	1000 pF	DC Block	Various	
R1 – R2	10 Ω	Res, 0402	Various	

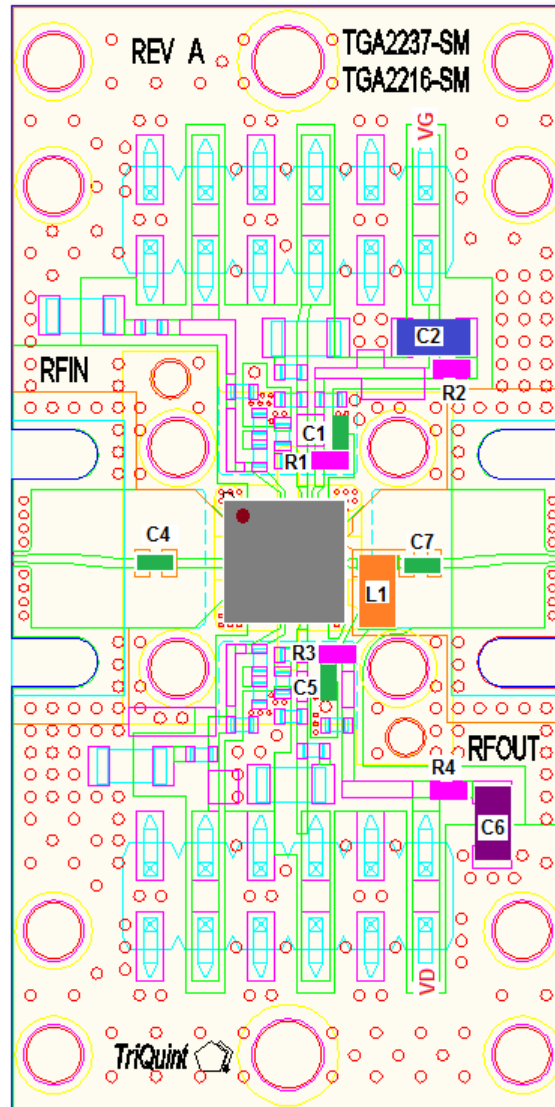
Application Circuit (Option with board-level DC blocks and output bias tee)



Notes:

1. Performance of the DUT with surface mount DC blocks and bias tee components may be degraded relative to the coaxial option. These components should be optimized for the desired operational bandwidth.

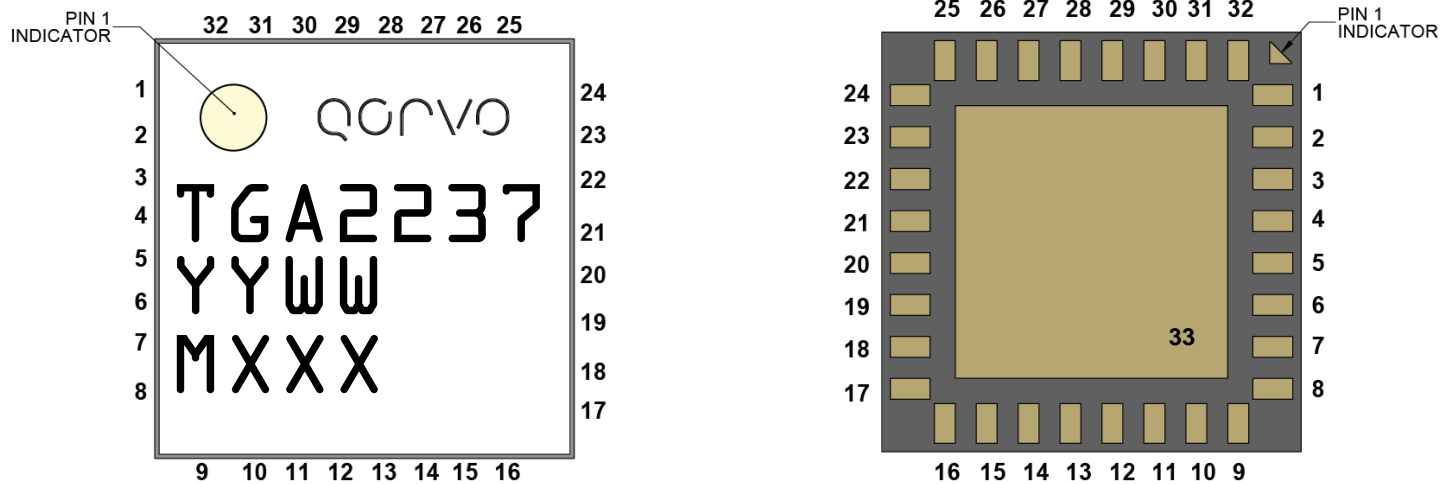
Evaluation Board Layout with On-Board DC Blocks and Output Bias-T Option



Bill of Materials For On-Board Bias-Tee

Reference Des.	Value	Description	Manuf.	Part Number
C1, C4, C5, C7	1000 pF	Cap, 0402, 100 V, 10%, X7R	Various	
C2	1 uF	Cap, 1206, 50 V, 10%, X7R	Various	
C6	0.01 uF	Cap, 1206, 100 V, 10%, X7R	Various	
L1	330 nH	Ind, 1206, 100 V, 10%, X7R	Various	
R1 – R4	10 Ω	Res, 0402	Various	

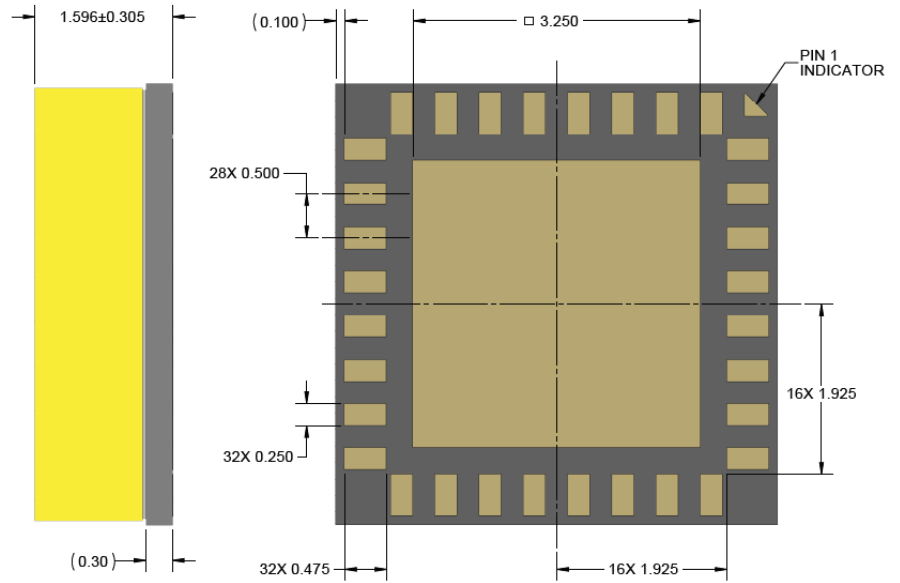
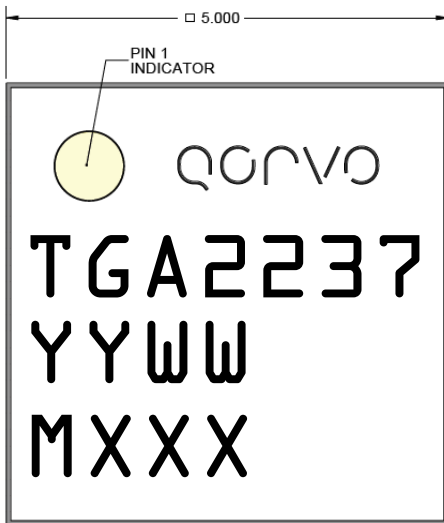
## Pin Layout



## Pin Description

Pad No.	Symbol	Description
1-2, 4, 6, 8-9, 16-17, 19, 21, 23-25, 32	GND	Connected to ground paddle (pin 33); must be grounded on PCB.
3, 7, 10-15, 18, 22, 27-31	NC	No connection.
5	RF IN	Input; matched to 50 $\Omega$ .
20	RF OUT/ DRAIN	Output; matched to 50 $\Omega$ . Drain voltage; bias network is required; see recommended Application Information on page 11 or 13.
26	GATE	GATE voltage; bias network is required; see recommended Application Information on page 11 or 13.
33	GND	Ground Paddle. Multiple vias should be employed to minimize inductance and thermal resistance.

Mechanical Information



Units: mm

Tolerances: unless specified

x.xx = ± 0.254

x.xxx = ± 0.127

Materials:

Base: Ceramic

Lid: Laminate

All metalized features are gold plated

Part is epoxy sealed

Marking:

2237: Part number

YY: Part Assembly year

WW: Part Assembly week

MXXX: Batch ID

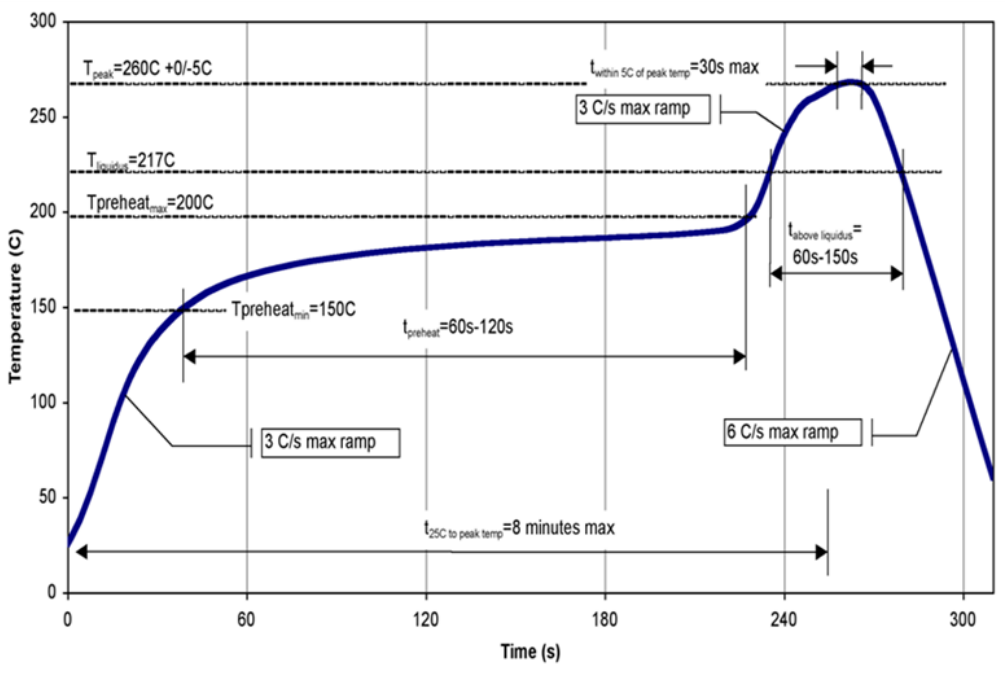


Assembly Notes

Compatible with lead-free soldering processes with 260°C peak reflow temperature.

Contact plating: Ni-Au.

Solder rework is not recommended.



Recommended Soldering Temperature Profile

## Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1C	ANSI/ESDA/JEDEC JS-001
ESD – Charge Device Model (CDM)	C2	ANSI/ESDA/JEDEC JS-002
MSL – Moisture Sensitivity Level	MSL 5a	IPC/JEDEC J-STD-020



Caution!  
ESD-Sensitive Device

## RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Antimony Free
- TBBP-A (C<sub>15</sub>H<sub>12</sub>Br<sub>4</sub>O<sub>2</sub>) Free
- PFOS Free
- SVHC Free

## Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

**Web:** [www.qorvo.com](http://www.qorvo.com)

**Tel:** 1-844-890-8163

**Email:** [customer.support@qorvo.com](mailto:customer.support@qorvo.com)

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